Roll No. | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 08

M.Tech. (Emb Sys) (2018 Batch) (Sem.–2)

ELECTRONIC SYSTEM DESIGN

Subject Code : MTES-PE3A-18

M.Code : 76211

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1.Attempt any FIVE questions out of EIGHT questions.

2.Each question carries TWELVE marks.

1. a) Design a 4-bit controlled complementary circuit that provides output equal to l's and 2's complement of input when the control input is logic '0' and T respectively.

   b) Design a 4-bit binary to gray code converter using logic gates.

2. a) How multiplexor can be used to realize different Boolean functions? Using 2:1 multiplexors, design a combinational logic with 3-inputs that provides output '1' when the inputs are greater than 3. The output is zero otherwise.

   b) Show that the characteristic equation of the JK flip-flop is Q(t+1)= JQ'+K'Q.

3. a) Design a 4-bit adder using full adder as a component in VHDL.

   b) Compare the VHDL over the Verilog hardware description language.

4. a) Write down the different steps of state reductions. Illustrate the advantages of state reduction.

   b) What is race condition in asynchronous finite state machine (FSM) designs? Explain race free assignment of states.

5. a) Draw the state diagram of the Mealy machine that provides high output when it detects a number which is divisible by four in the latest three bits of the input sequence. The overlapping is allowed for this problem.

   b) Write the difference between synchronous and asynchronous designs. Also write short notes on hazards and essential hazards.

6. Implement the following Boolean expressions using PAL :

   $w(A, B, C, D) = \Sigma (2,12,13)$,

   $x(A, B, C, D) = \Sigma (7,8,9,10, 11,12,13,14,15)$,

   $y(A, B, C, D) = \Sigma (0,2,3,4,5,6,7,8,10,11,15)$, and

   $z(A, B, C, D) = \Sigma (1,2,8,12,13)$.

7. a) Write down the different steps to design an asynchronous finite state machine (FSM).

   b) What are prime timing issues we considered in the static timing analysis of sequential digital circuit? How these issues can be addressed?

8. a) Compare a digital circuit when implemented using ROM, PLA and PAL on the basis of implementation area, configurability and ease of implementation.

   b) Discuss the activity involved in the system development life cycle. Discuss why system feasibility study is essential in the system analysis and design?

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.