Roll No. | | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 08

M.Tech. (Microelectronics) (Sem.–1)

ELECTRONIC SYSTEM DESIGN

Subject Code : ME-803

M.Code : 38403

Time : 3 Hrs. **Max. Marks : 100**

INSTRUCTIONS TO CANDIDATES :

1. **Attempt any FIVE questions out of EIGHT question.**
2. **Each question carries TWENTY marks.**

Ql. (a) Design 2- input XOR gate using 2:1 multiplexer.

(b) Design full adder using half adders.

Q2. (a) Draw the output timing diagram of a rising edge-triggered D Flip Flop, given the following input (D) and clock (CLK) signals in Fig. 1.

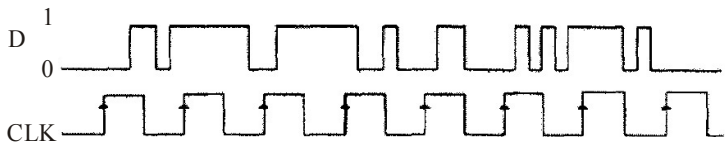

Figure. 1

(b) Differentiate between asynchronous and synchronous digital design. Name the asynchronous signals (with their functions) used in the flip flops.

Q3. (a) Draw the state diagram of J-K flip-flop.

(b) What is clock Skew and why clock skew is a problem?

Q4. (a) What are different ways to synchronize between two clock domains?

(b) What is difference between PLA and PAL?

Q5. What is the main purpose of using MSI decoders and multiplexers in system controller design? Discuss in detail.

Q6. What is electromagnetic interference in digital circuits and how to avoid it?

Q7. What is indirect addressed multiplexers configurations? Discuss in detail.

Q8. Short notes **(any two) :**

(a) Electromagnetic compatibility grounding

(b) Tri-State Bus System

(c) Hazards

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.