Roll No. | | | | | | | | | | | | | Total No. of Pages : 01

Total No. of Questions : 08

M.Tech.(VLSI D) (2016 & Onwards) (Sem.–2)

ALGORITHMS FOR VLSI DESIGN AUTOMATION

Subject Code : MTVL-201

M.Code : 74258

Time : 3 Hrs. Max. Marks : 100

INSTRUCTIONS TO CANDIDATES :

1. Attempt any FIVE questions out of EIGHT questions.
2. Each question carries TWENTY marks.

Q1. Discuss in detail about the Hardware models for High-level synthesis. Also explain the Binary decision diagram in detail.

Q2. a) Explain the Group migration algorithms in VLSI design automation.

b) Discuss the simulated annealing and evolution in VLSI design automation.

Q3. Discuss in detail about the floor planning algorithms for mixed block and cell design. Also explain the general and channel pin assignment.

Q4. Explain the Line probe algorithm in VLSI design automation. Also discuss the Maze routing algorithm in detail.

Q5. a) Discuss the three layer channel routing algorithms in VLSI design automation.

b) Discuss the switchbox routing algorithms.

Q6. What type of minimum distance rules used in VLSI design? Explain the type of problems present in placement with examples.

Q7. Explain the problems associated during routing in gate array design process. Also discuss the channel routing problems.

Q8. What are the important entities for VLSI design? Explain the various optimization problems in floor planning.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.