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M.Tech. (VLSI D) (2016 & Onwards) (Sem.-2) TESTING AND FAULT TOLERANCE

Subject Code: MTVL-202 M.Code: 74259

Time: 3 Hrs. Max. Marks: 100

INSTRUCTIONS TO CANDIDATES:

- 1. Attempt any FIVE questions out of EIGHT questions.
- 2. Each question carries TWENTY marks.
- 1. a) Discuss the role of testing in VLSI circuits.
 - b) Explain the basic principle of digital testing.
- 2. a) Explain functional testing and structural testing with the help of a suitable example.
 - b) What do you understand by fault modeling? Explain behavioural fault.
- 3. Write short notes on:
 - a) Fault Dominance
 - b) Spatial redundancy
- 4. What is concurrent fault simulation? Explain with the help of an example.
- 5. Perform ATPG for the fault line h s-a-1 in the circuit of Figure 1 using PODEM and SCOAP measures.

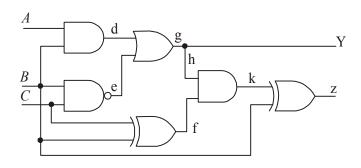


FIG.1

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6. Determine a test sequence for the s-a-0 fault on the output line of the flip-flop in the circuit of Figure 2.

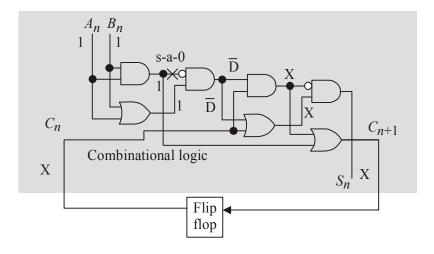


FIG.2

- 7. Discuss the various scan design rules.
- 8. Discuss pseudo-random pattern generation for BIST.

NOTE: Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.

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