

6. Determine a test sequence for the s-a-0 fault on the output line of the flip-flop in the circuit of Figure 2.

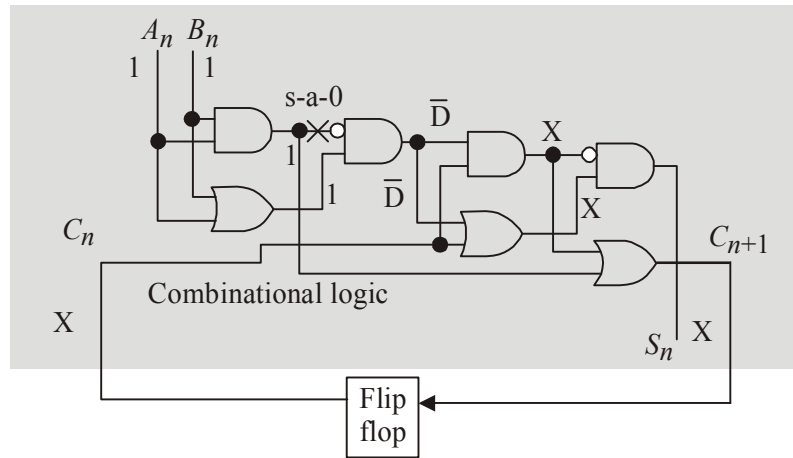


FIG.2

7. Discuss the various scan design rules.
8. Discuss pseudo-random pattern generation for BIST.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.