Roll No. ☐☐☐☐☐☐☐☐☐☐☐☐☐   Total No. of Pages : 02

Total No. of Questions : 08

M.Tech. (VLSI D) (2018 Batch) (Sem.–2)
ANALOG DIGITAL & MIXED SIGNAL CMOS DESIGN
Subject Code : MTVL-103-18
M.Code : 76197

Time : 3 Hrs.   Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :
**1.Attempt any FIVE questions out of EIGHT questions.**
**2.Each question carries TWELVE marks.**

Q.l   (a) Draw voltage transfer characteristics of CMOS inverter and derive expression for V_{IL}, V_{IH}, V_{OL} and V_{OH}.

       (b) Implement 4:1 MUX using pass transistor logic and transmission gate logic.

Q.2   (a) Briefly explain cascaded domino CMOS logic circuit for high performance dynamic logic circuit.

       (b) For the circuit below, What are the activity factors of nodes X, Y, Z and OUT if P $(A = l) = P (B = l) = P (C = l) = 0.5$?
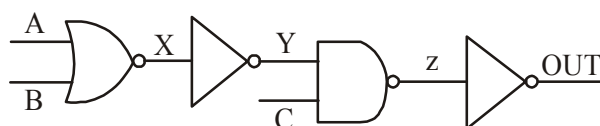
Q.3   (a) Draw the circuit diagram for CMOS two-input NAND gates and explain its operation.

       (b) Draw the stick diagram for CMOS two-input NOR gate.

Q.4   (a) Design a CMOS clocked SR tlip flop and explain its operation.

       (b) Draw and explain the operation of C^2 MOS master slave positive edge triggered register.

Q.5   (a) Why is emitter resistance R_E replaced by a constant current bias circuit in differential amplifier stage of an op-amp?

       (b) An active-loaded MOS differential pair as shown in Fig. 2 is specified as follows :

$$\left(\frac{W}{L}\right)_n = 100. \left(\frac{W}{L}\right)_p = 200, \mu_n C_{ox} - 2\mu_p C_{ox} = 0.2mA/V^2, V_{An} = |V_{Ap}| = 20\,V, I = 0.8mA, Rss = 25k\Omega.$$
.

Calculate G_m, R_0, A_d, $|A_{cm}|$ and CMRR.
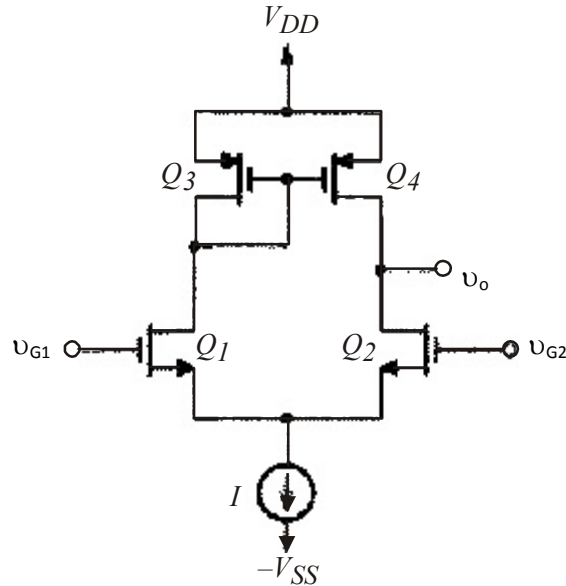
Q.6 (a) Draw a standard cascode current sink circuit and explain its operation and output characteristics.

   (b) Explain why the Gilbert cell can operate as an analog voltage multiplier.

Q.7 (a) Explain the principle of Miller Compensation of two stage op-amp.

   (b) Design an op-amp with ideal op-amp characteristics. Explain the steps, conditions and requirements to design an op-amp.

Q.8 Write short notes on any **two** of the following :

   (a) FinFET

   (b) Non-bistable sequential circuit

   (c) Speed and power dissipation in dynamic logic

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.