Roll No. | | | | | | | | | | | | | Total No. of Pages : 01

Total No. of Questions : 08

M.Tech. (VLSI D) (2018 Batch) (Sem.–2)

LOW POWER VLSI DESIGN

Subject Code : MTVL-PE3A-18

M.Code : 76199

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1.Attempt any FIVE questions out of EIGHT questions.

2.Each question carries TWELVE marks.

1. What are the sources of power dissipation in digital ICs? Derive the equation for short circuit power dissipation in a CMOS inverter.

2. a) Write a short note on drain induced barrier lowering.

   b) Explain basic principles of low power design.

3. Discuss methods of estimating average power in combinational circuits.

4. Explain in detail about power dissipation in clock distribution.

5. Explain the various sources and reduction of power dissipation in memory subsystem.

6. a) Explain the various factors essential for software power estimations.

   b) Explain the software power estimation with suitable example.

7. a) Compare between VTCMOS and MTCMOS for leakage power reduction.

   b) Design an adiabatic two input AND/NAND gate.

8. Short notes (any **TWO**) :

   a) Power management support

   b) Zero skew versus tolerable skew

   c) Single driver versus distributed buffers

   d) Low power SRAM circuits

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.