Roll No. | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 18

B.Tech. (ECE) (2018 Batch) (Sem.–3)

DIGITAL SYSTEM DESIGN

Subject Code : BTEC-302-18

M.Code : 76445

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

Write briefly :

1. Define the term Entity.
2. What is an Array?
3. What is Combinational Circuits?
4. List out the elements present in the ASM chart.
5. Write down the features of FPGA.
6. Write the Verilog code for half adder using gate level modelling.
7. "*PAL has reprogrammable AND array, whereas GAL has programmable AND array*". Comment.
8. Define Speed Power Product. What is its significance?
9. Define fan-in, fan-out.
10. What is race around condition?

SECTION-B

11. Design and summarize the internal 3 sections of LS-TTL NAND gate and analyze the circuit with the help of function table.

12. Design 1-bit comparator using 2-4 decoder giving three output G, E and L.

13. Applying a 4-bit shift register, design a 4-bit twisted ring counter.

14. Explain various data types available in VHDL.

15. Implement a T-FF with active low asynchronous inputs and clock inputs in VHDL.

SECTION-C

16. Design a serial adder Moore type FSM.

17. List out the steps to be consider for PLA folding algorithm.

18. How a sequential circuit can be designed using FPGA?

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.