Roll No. | | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 09

B.Tech.(ECE) (2018 Batch) (Sem.–3)

DIGITAL SYSTEM DESIGN

Subject Code : BTEC-302-18

M.Code : 76445

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Write briefly :

a) What is the operational difference between SRAM and DRAM?

b) How merged table be transformed into the excitation table?

c) What are combinational circuits?

d) Find the min-terms of the logic expression Y= A'B'C'+A'B'C+A'BC+ABC'.

e) Draw the logic diagram of SR latch using NOR gate.

f) What is single slope A/D converter?

g) Write the names of different modelling of VHDL.

h) Draw state diagram of 3-bit modulo 6 binary counter.

i) Explain the concept of binary cell.

j) State noise figure and figure of merit.

SECTION-B

2. List the predefined types for signal declaration in VHDL.

3. Explain Moore's and Melay sequential circuit.

4. Draw and explain the CPLD in detail.

5. Explain and provide the characteristics table, characteristic equation and excitation table for D-flip flop and J-K flip flop.

6. Describe the steps to design output Decoder along with the example.

SECTION-C

7. Realize the function $F(A,B,C,D) = \Sigma\, m(0,2,5,7,8,10,11,14)$ using PAL.

8. Describe cycles and races in asynchronous FSM along with the example.

9. Design full adder using structural modelling in VHDL.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.