Roll No. | | | | | | | | | | | | | Total No. of Pages : 01

Total No. of Questions : 08

M.Tech.(VLSI D) (2016 & Onwards) EL-III (Sem.–2)

# LOW POWER VLSI DESIGN

Subject Code : MTVL-209

M.Code : 74265

Time : 3 Hrs. Max. Marks : 100

**INSTRUCTIONS TO CANDIDATES :**

1. **Attempt any FIVE questions out of EIGHT questions.**
2. **Each question carries TWENTY marks.**

1. a. What is the need of low power VLSI chips? Explain the impact of technology on scaling. 10
   b. Derive an expression for short circuit power dissipation of a CMOS inverter. 10
2. a. Explain the circuit level technique for minimization of power dissipation. 12
   b. How dynamic dissipation in CMOS effect the performance of the device? 8
3. With neat diagrams explain the dual bit type signal model for DSP system. Explain how data path module is characterized for a module with one input and one output such as FIFO queue, with relevant capacitance and power expression? 20
4. a. Explain about the modelling and analysis of a transistor using SPICE. 10
   b. Give the expression for entropy. Discuss the entropy based power estimation method. 10
5. a. With circuit examples, explain the difference transformation methods used for gate reorganization. 10
   b. Explain the concept of bus invert encoding with relevant expressions. 10
6. a. With an illustration control data flow graph and hardware architecture, explain the flow graph transformation with operation reduction. 10
   b. Explain guarded evaluation technique to reduce switching activities. 10
7. a. Explain the concept of buffer insertion in an equal path length clock tree using balance buffer insertion. 10
   b. Explain guarded evaluation technique to reduce switching activities. 10
8. With a neat block diagram, explain the design flow at algorithm level. Describe the architecture level estimation and synthesis. 20

**NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student**.