

Roll No.

Total No. of Pages : 02

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M.Tech. (VLSI D) (2018 Batch) (Sem.-2)
VLSI DESIGN VERIFICATION & TESTING
Subject Code : MTVL-104-18
M.Code : 76198

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. Attempt any FIVE questions out of EIGHT questions.
2. Each question carries TWELVE marks.

1. a) Write down the basic test bench functionality with the help of its block diagram. (6)
b) Explain directed testing and compare its progress with the random testing. (6)
2. a) How new data-types are created in System Verification? Explain enumerated types with suitable example. (6)
b) Discuss guidelines for choosing the right storage types in SystemVerilog. (6)
3. a) Define the various physical faults model using example. (6)
b) Write short notes on fault equivalence and fault collapsing. (6)
4. a) For a two-input AND gate and a two-input Exclusive-OR gate, develop
i. The singular cover of the gates (3)
ii. The propagation D-cubes (3)
iii. Primitive D-cubes of failure for a sa1 fault on one of the gate inputs. (2)
b) Explain how testing can evaluate redundancy in the design. (6)

5. For the circuit of Figure 1:
- Enumerate the minimal set of single stuck-at faults that must be tested according to the Checkpoint Theorem. (6)
 - Show that the two faults d s-a-0 and g s-a-1 are equivalent. (6)

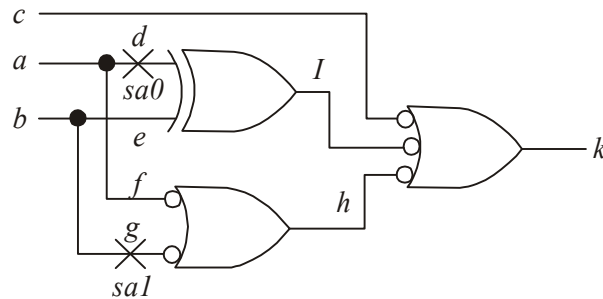


Figure 1: Combinational circuit with stuck-at faults.

- Explain and compare serial and parallel fault simulation methods. (6)
 - Explain what action an event-driven true-value simulator will take when it evaluates a zero-delay gate. (6)
- Explain BIST? Describe logic BIST random and weighted random pattern testability. (6)
 - Describe full and partial scan design for sequential circuits. (6)
- Draw the TAP controller state diagram and timing diagrams. (6)
 - What is the advantage of weighted pseudo random pattern generator over the normal method? (6)

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.